IN THE TITLE OF THE INVENTION:

Please DELETE the Title of the Invention in its entirety and substitute with the following:

- - SEMICONDUCTOR INTEGRATED CIRCUIT TIMING ANALYSIS APPARATUS, TIMING ANALYSIS METHOD AND TIMING ANALYSIS PROGRAM - -

IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE the paragraph beginning at page 28, line 18, with the following paragraph:

In Fig. 7, reference numeral 71 denotes a timing analysis unit-A, which performs timing analysis of the target path by accumulating the variation in delay of each gate in the path which is an analysis target (target path). Reference numeral 72 denotes a determination unit, to which the analysis result of the timing analysis unit-A 71 is supplied, and which determines whether the target path satisfies previously specified timing conditions (conditions relating to the setup time and hold time). The determination unit 72 outputs the determination result to a result output unit 38, and outputs the information relating to the path which does not satisfy the timing conditions to the coefficient arithmetically operating unit 33. A timing analysis unit-B 37 constitutes a ~~first~~ second timing analysis unit of the present invention, and the timing analysis unit-A 71 constitutes a ~~second~~ first timing analysis unit of the present invention.